Connect 4

Simulating Several Electric Motors with the DS1006 Quad-Core

When applications demand especially high processing power from a simulator, parallelization is often the answer. Hybrid drives are a typical example. A minimal model sampling rate is vital for simulating electric motors because it determines how precise and stable the engine control can be. This is the perfect playground for quad-core processors.

Applications and Advantages

When electric drives are simulated, the scenarios often require simultaneous calculation of several complex simulation models in real time. This includes hybrid drives, diesel-electric drives in commercial vehicles and locomotives, and path control of multi-axle drives in industrial machines. There are also applications in aeronautics, as when hydraulic actuators are replaced with electric motors.

Executing these computation-intensive simulations on one single processor board has many decisive advantages over using several boards:

- Higher bandwidth and lower latencies for communicating between models
- Flexible power reserves for further submodels to easily expand the simulator if necessary
- Attractive price/performance ratio

Quad-Power

The dSPACE DS1006 Processor Board with an AMD Opteron™ Quad-Core Processor (2.8 GHz) was designed exactly for this power range. Together with dSPACE's I/O solutions for electric motors, it supports the setup of hardware-in-the-loop (HIL) simulators that test the controllers of electric and hybrid drives. Each of the four cores can calculate a simulation model, so an internal combustion engine model and three electric engine models can be simulated simultaneously, or one internal-combustion engine model, two electric engine models, and a rest-bus simulation model or transmission model, and so on.

Communication between Processor Cores

The efficiency of the processor-internal communication is another vital factor, and high bandwidth and low latency are key. The cores of the

Signals for the Simulation
To test the ECUs of drive motors, it is usually sufficient to evaluate the signal level of the power electronics. To do so, the power electronics are removed, and only the signal processing portion of the ECU is connected to the simulator.

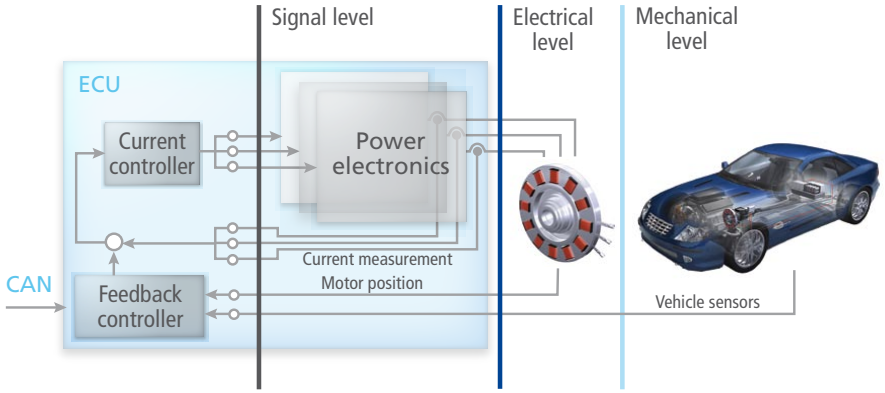


Figure 1: Interfaces for electric motor simulation.

quad-core DS1006 Processor Board communicate via virtual Gigalink connections. These have over 100 times the throughput and only a tenth of the latency of the optical Gigalink connections between the single-core DS1006 Processor Boards.

RTI models for DS1006 boards can be reused easily with the new quad-core DS1006. Another advantage for scaling is the data throughput of the optical Gigalink connection, which is twice as high as that of the previous single-core DS1006.

Graphical configuration for easily assigning models to the processor cores.

These figures apply to transfers of large data amounts between several cores of the quad-core processor on a quad-core DS1006. The figures are even better with smaller volumes of data.

Graphical Configuration with RTI-MP

The Real-Time Interface for Multiprocessor Systems (RTI-MP) software is used to configure the virtual Gigalink connection. In Simulink®, the blocks used for optical Gigalinks are the same as those used for virtual Gigalinks. This explains why the graphical representations of multi-core and multiprocessor configurations are identical. This versatility simplifies the scaling of processing power and I/O performance. Existing

Model Distribution and I/O Configuration

To fulfill the diverse test requirements for electric motors, the simulation models and I/O models can be distributed flexibly on the processor cores of the quad-core DS1006. Figure 2 shows a typical simulation model distribution and I/O distribution for testing hybrid drives. The first core calculates the model of the internal combustion engine. This is the main task of the multiprocessor (MP) model. The second core and third core execute the model (synchronous motor and inverter) and I/O access for the electric motor, respectively. The fourth core is free for further models, such as for simulating restbus communication. It can also execute the model and the I/O access of a third electric motor, for example, to simulate an auxiliary drive like a starter or a pump.

I/O Interfaces for Hybrid Drives

In the example shown in Figure 2, a dSPACE Electric Motor HIL (EMH) Solution is used for each electric motor. The EMH Solution is based on a dSPACE DS5202 FPGA Base Board and offers all the necessary I/O channels for simulating up to two electric motors. This includes outputting and measuring PWM signals and emulating the position sensor signals. The EMH Solution's I/O access is performed by the appropriate models on the 2nd and 3rd cores of the processor. The DS2211 HIL I/O Board covers the I/O requirements of the internal-combustion engine that is calculated on the first core of the processor. And there are separate PWM and PSS Solutions to cover especially extensive I/O requirements. These I/O boards were already been used with the quad-core DS1006 to develop a complete vehicle platform for solid models with a hybridized drivetrain.

Short Sample Times

With the model distribution used in the hybrid example, the control loops of all simulated electric motors

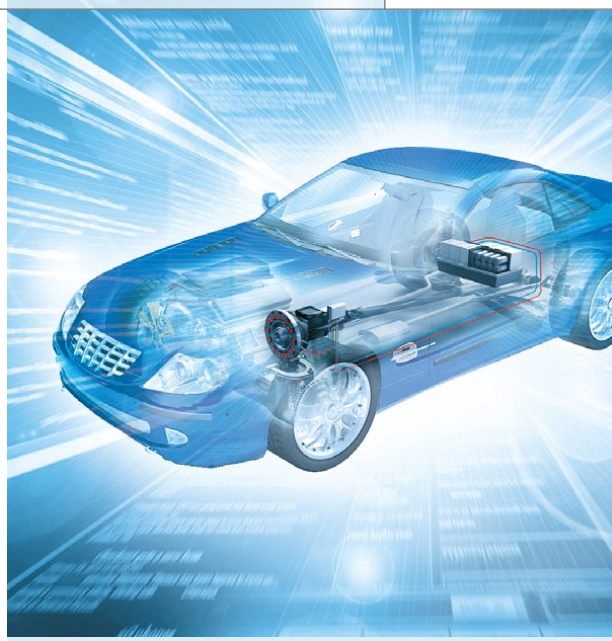
can still be calculated accurately at sample rates (PWM control frequencies) of 25 kHz. And there is still enough reserve capacity for handling additional I/O requirements and model requirements.

Precise Signal Measurement and Emulation

With a 3-phase PWM generated by the electronic control unit, the measurements of all the important control signal times for the power stages (duration of the PWM signal and the high- and low-side signals, and the dead time) are highly accurate. The measurements are carried out pulse-center-aligned to the PWM signals, with a resolution of 25 ns. The interrupts for the real-time model of the electric motor are also generated center-aligned to the control signals. The speed signals and position signals of the various analog (resolver, encoder) and digital (incremental encoder) sensor types are precisely simulated with a time resolution of 100 ns and 25 ns, respectively.

Summary

With the quad-core DS1006 Processor Board, equipped with an AMD Opteron™ Quad-Core Processor (2.8 GHz), up to three electric motors can be simulated to test electronic control units. This configuration is especially interesting for ECU tests of hybrid drives. The entire drivetrain can be simulated on a quad-core DS1006, including the models of the internal-combustion engine and the transmission. The signals necessary for carrying out simulations are made available via tailor-made I/O interfaces. ■



In Brief

- Precise real-time simulation of hybrid drives on one board
- Simultaneous simulation of up to three electric motors, including the internal-combustion engine model and transmission model
- High-performance I/O interfaces for electric motor signals

Figure 2: Each of the four processor cores of the quad-core DS1006 can calculate a model. With two electric motor models and an internal-combustion engine model, including the transmission, there is still one core available for restbus simulation or as a reserve core.